A 10.5 mΩ, 4 A Integrated Power Switch with Soft-start and Protection Features in WLCSP

General Description

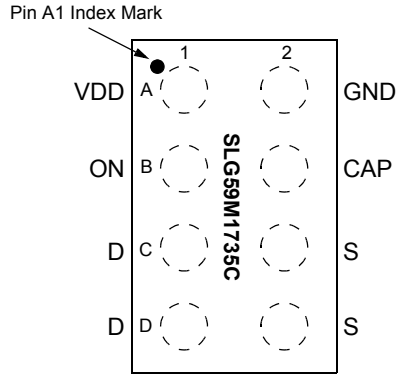
The SLG59M1735C is a high performance 10.5 mΩ, 4 A single-channel nFET integrated power switch which can operate with a 2.5 V to 5.5 V V_{DD} supply to switch power rails from as low as 0.9 V up to the supply voltage. The SLG59M1735C incorporates two-level overload current protection, thermal shutdown protection, and soft-start control which can easily be adjusted by a small external capacitor.

Using a proprietary MOSFET design, the SLG59M1735C achieves its stable 10.5 mΩ RDS_{ON} across a wide input voltage range. Through the application of Silego's proprietary CuFET technology, the SLG59M1735C's can be used in high-current applications with a very-small 1.5 mm^2 WLCSP form factor.

Features

- Low RDSON nFET: 10.5 mΩ
- Steady-state Operating Current: Up to 4 A
- Supply Voltage: 2.5 V ≤ V_{DD} ≤ 5.5 V
- Wide Input Voltage Range: 0.9 V ≤ V_D ≤ V_{DD}
- Capacitor-programmable Soft-start Control
- Two-stage Overcurrent Protection:
  - Fixed 6 A Active Current Limit
  - Fixed 0.5 A Short-circuit Current Limit
- Thermal Shutdown Protection
- Operating Temperature: -40 °C to 85 °C
- 0.96 mm x 1.56 mm, 0.4mm pitch 8L WLCSP
  - Pb-Free / Halogen-Free / RoHS-Compliant

Pin Configuration

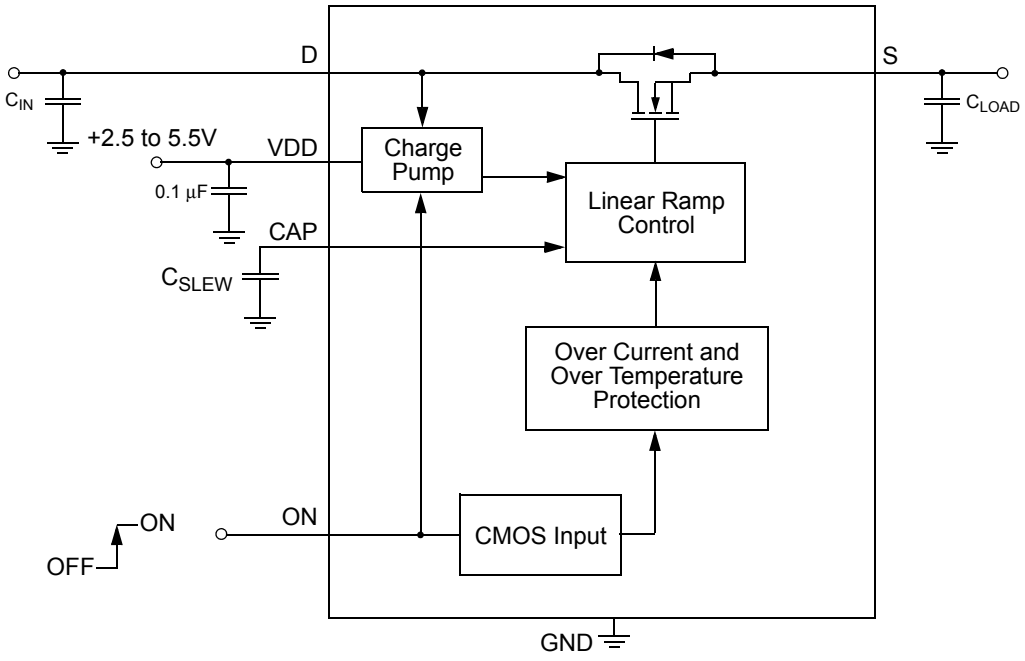


8-pin WLCSP
(Laser Marking View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A1	VDD	PWR	V_{DD} power for load switch control (2.5 V to 5.5 V)
B1	ON	Input	Turns MOSFET ON (4 MΩ pull down resistor) CMOS input with V_{IL} < 0.3 V, V_{IH} > 0.85 V
C1	D	MOSFET	Drain of Power MOSFET (fused with pin 4)
D1	D	MOSFET	Drain of Power MOSFET (fused with pin 3)
D2	S	MOSFET	Source of Power MOSFET (fused with pin 6)
C2	S	MOSFET	Source of Power MOSFET (fused with pin 5)
B2	CAP	Input	Capacitor for controlling power rail ramp rate
A2	GND	GND	Ground

Ordering Information

Part Number	Type	Production Flow
SLG59M1735C	WLCSP 8L	Industrial, -40 °C to 85 °C
SLG59M1735CTR	WLCSP 8L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
T_S	Storage Temperature		-65	--	150	°C
T_O	Operating Temperature		-40	--	85	°C
T_A	Rated Operating Temperature		-40	--	85	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	4	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	6	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	0.96mm x 1.56mm WLCSP; Determined using 1 in^2, 1 oz. copper pads under each VD and VS on FR4 pcb material	--	100	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1	W
IDS_{MAX}	Max Continuous Switch Current		--	--	4	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-40 to 85°C	2.5	--	5.5	V
I_{DD}	Power Supply Current	when OFF	--	--	2	µA
		when ON	--	77	110	µA
RDS_{ON}	ON Resistance	T_A 25°C @ 100 mA; V_{DD} = V_D = 5 V	--	10.5	12.1	mΩ
		T_A 85°C @ 100 mA; V_{DD} = V_D = 5 V	--	12.7	14.3	mΩ
V_D	Drain Voltage		0.9	--	V_{DD}	V
I_{FET_OFF}	MOSFET OFF Leakage Current	2.5V ≤ V_{DD} ≤ 5.5V; V_D = 4.35V, V_S = 0V; ON = LOW; T_A = 25°C	--	--	1	µA
I_{LIMIT}	Active Current Limit	MOSFET will automatically limit current when V_S > 250 mV	4.5	6.0	8	A
	Short Circuit Current Limit	MOSFET will automatically limit current when V_S < 250 mV	--	0.5	--	A
T_{ON_Delay}	ON Delay Time	50% ON to 10% V_S ↑; V_{DD} = V_D = 5 V; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	--	220	400	µs
$V_{S(SR)}$	Slew Rate	10% V_S to 90% V_S ↑;	Set by External C_{SLEW}[1]			µs
		Example: 10% V_S to 90% V_S ↑; V_{DD} = V_D = 5 V; C_{SLEW} = 3.9 nF R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	2.2	2.8	3.5	V/ms

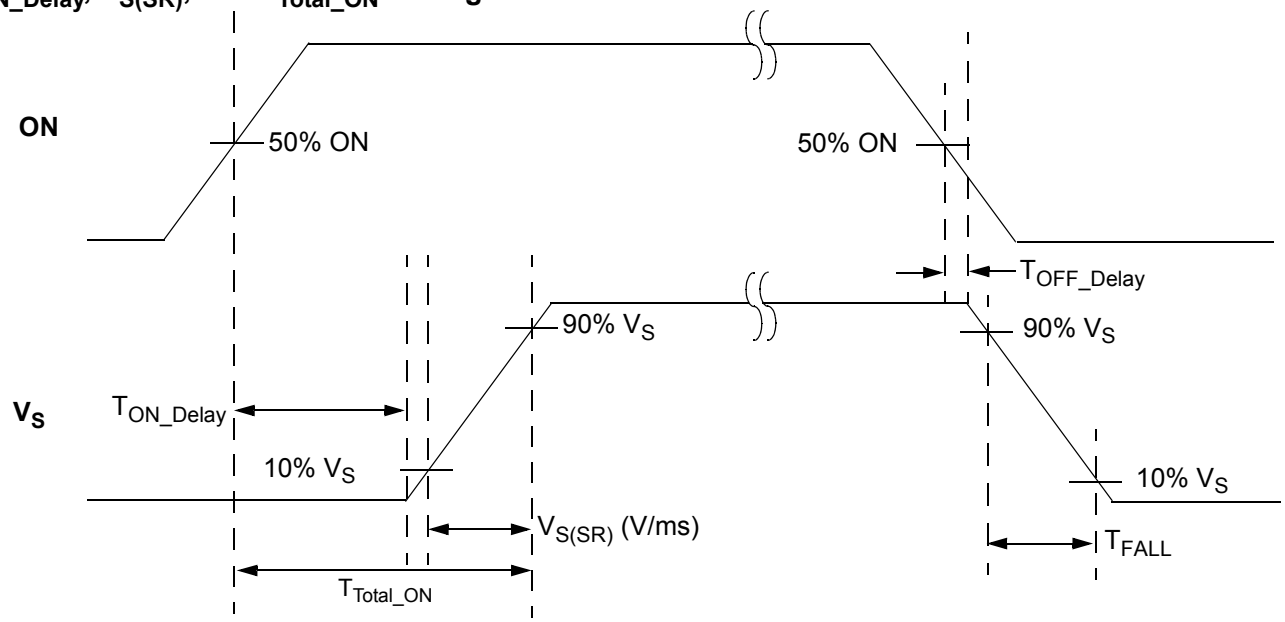
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{Total_ON}	Total Turn-on Time	50% ON to 90% V_S ↑	Set by External C_{SLEW}[1]			ms
		Example: 50% ON to 90% V_S ↑ V_{DD} = V_D = 5 V; C_{SLEW} = 3.9 nF R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	1.5	1.9	2.3	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S ↓; V_{DD} = V_D= 5 V, R_{LOAD} = 20 Ω, no C_{LOAD}	--	23	--	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from V_S to GND	--	--	500	µF
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C

Notes:
1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.

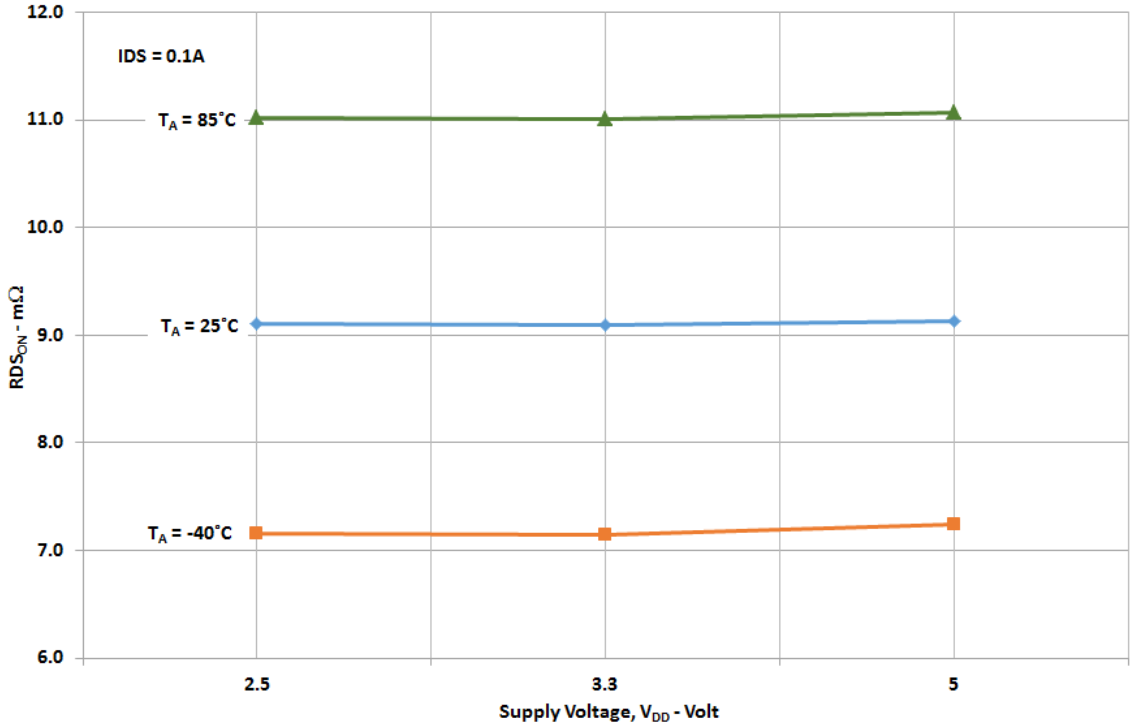
T_{ON_Delay}, $V_{S(SR)}$, and T_{Total_ON} Timing Details



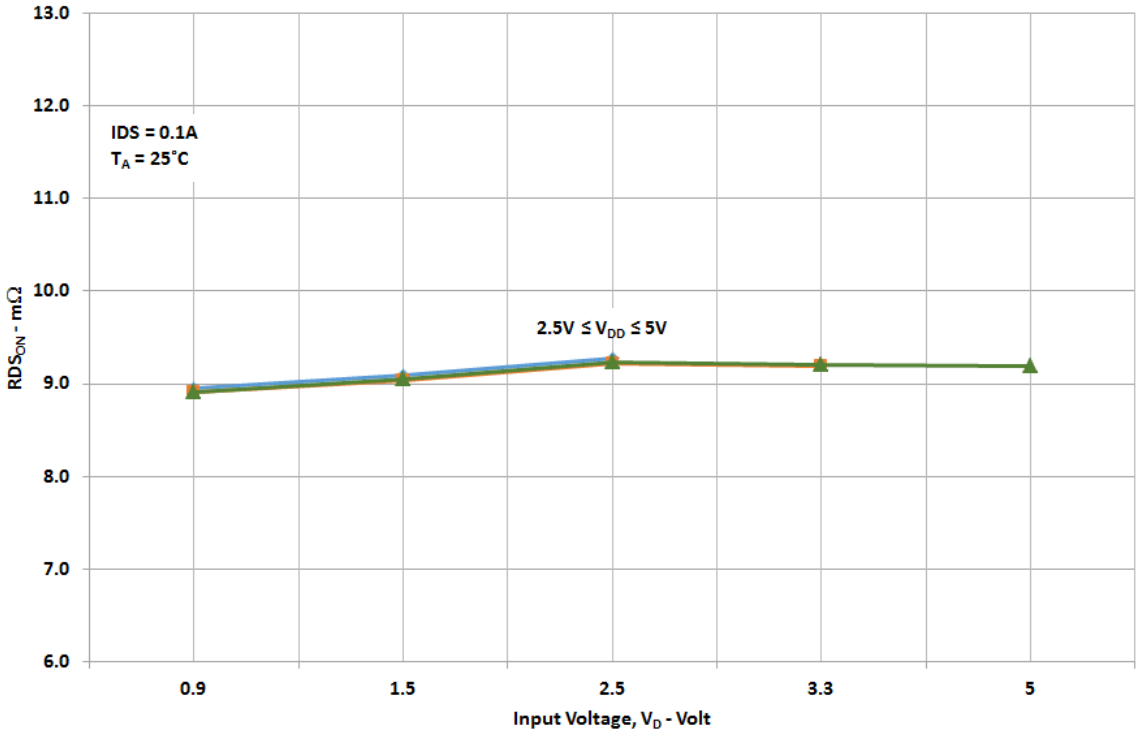
Note: Rise and Fall times of the ON signal are 100 ns

Typical Performance Characteristics

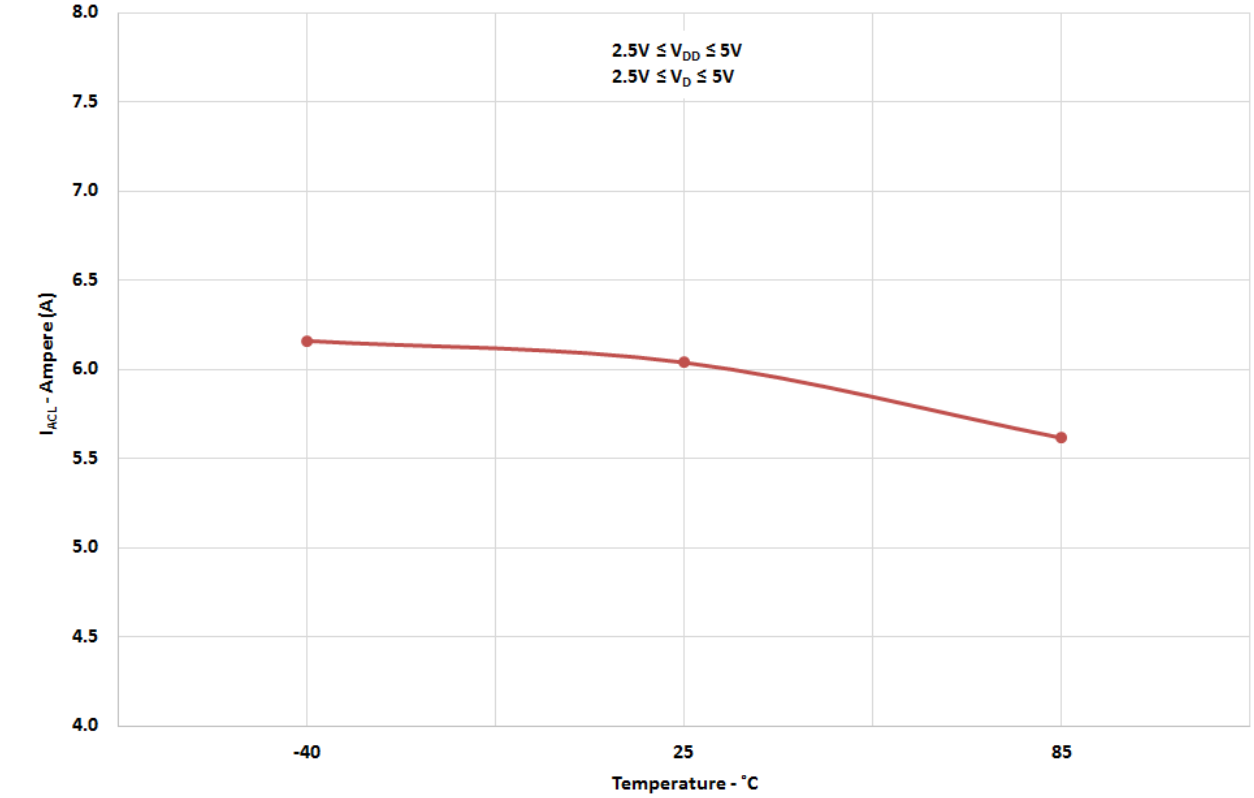
RDS_{ON} vs. V_{DD} and Temperature



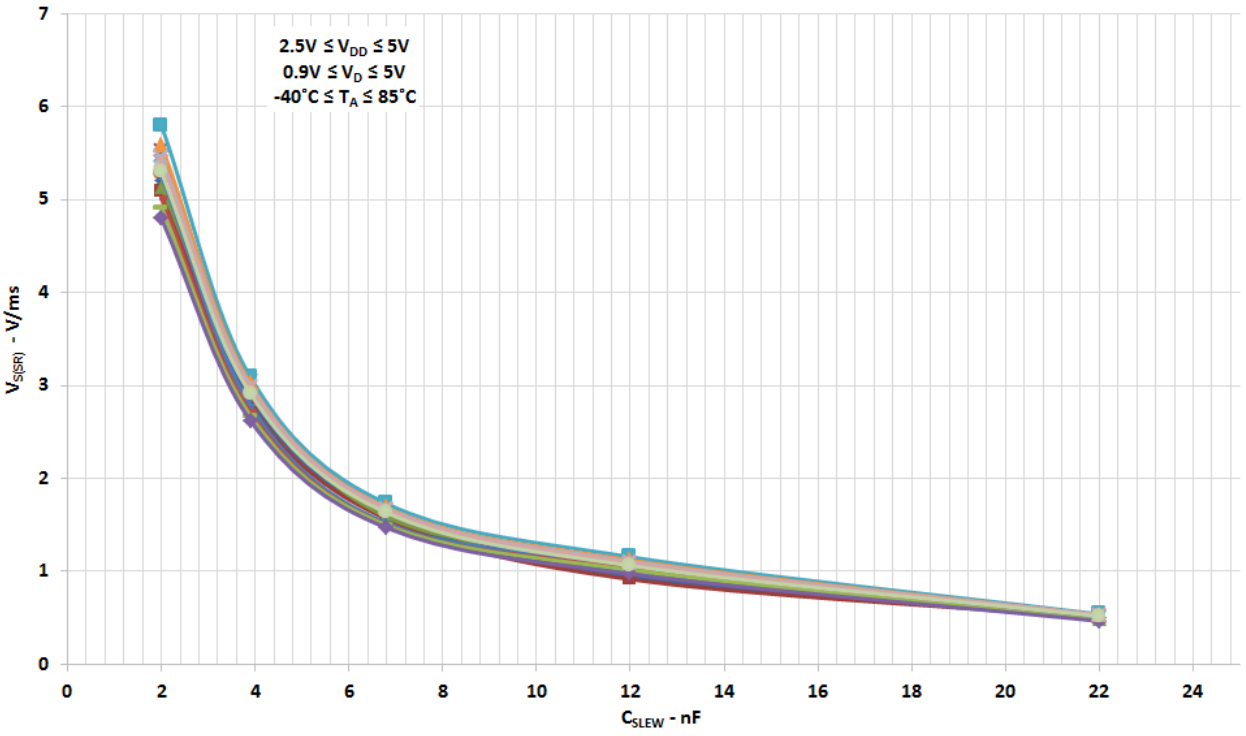
RDS_{ON} vs. V_D and V_{DD}



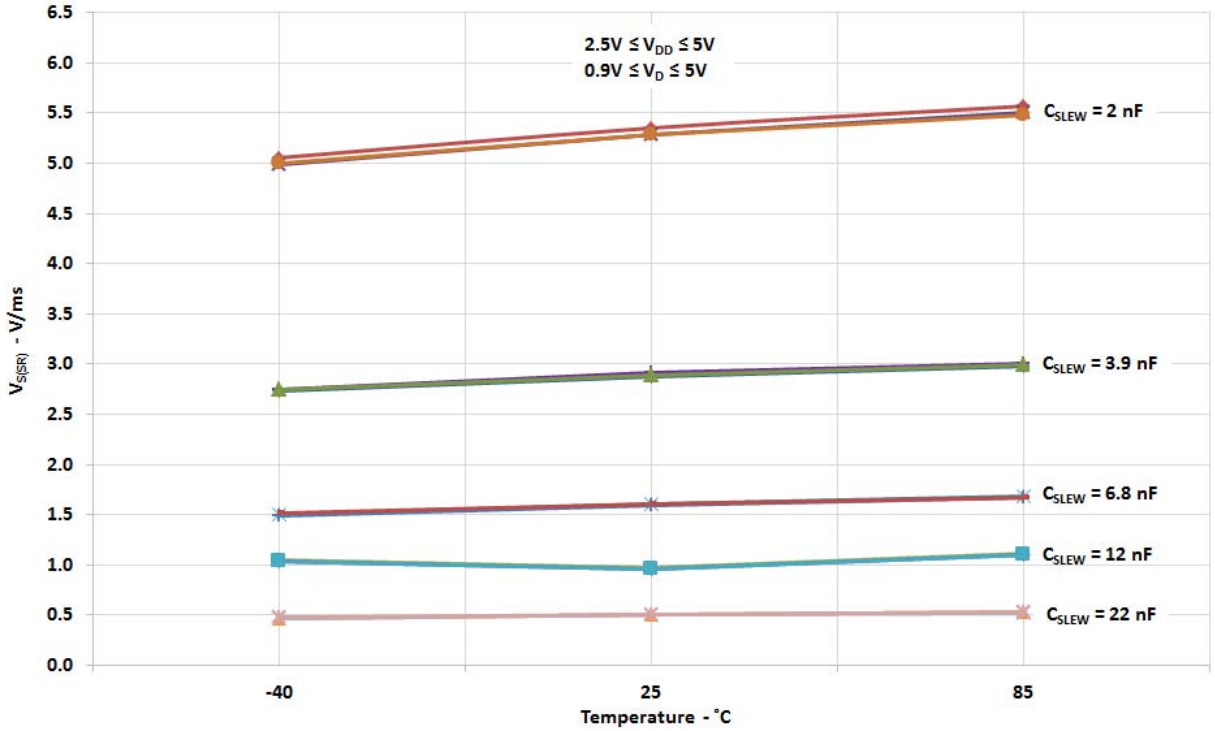
I_{ACL} vs. Temperature, V_{DD}, and V_D



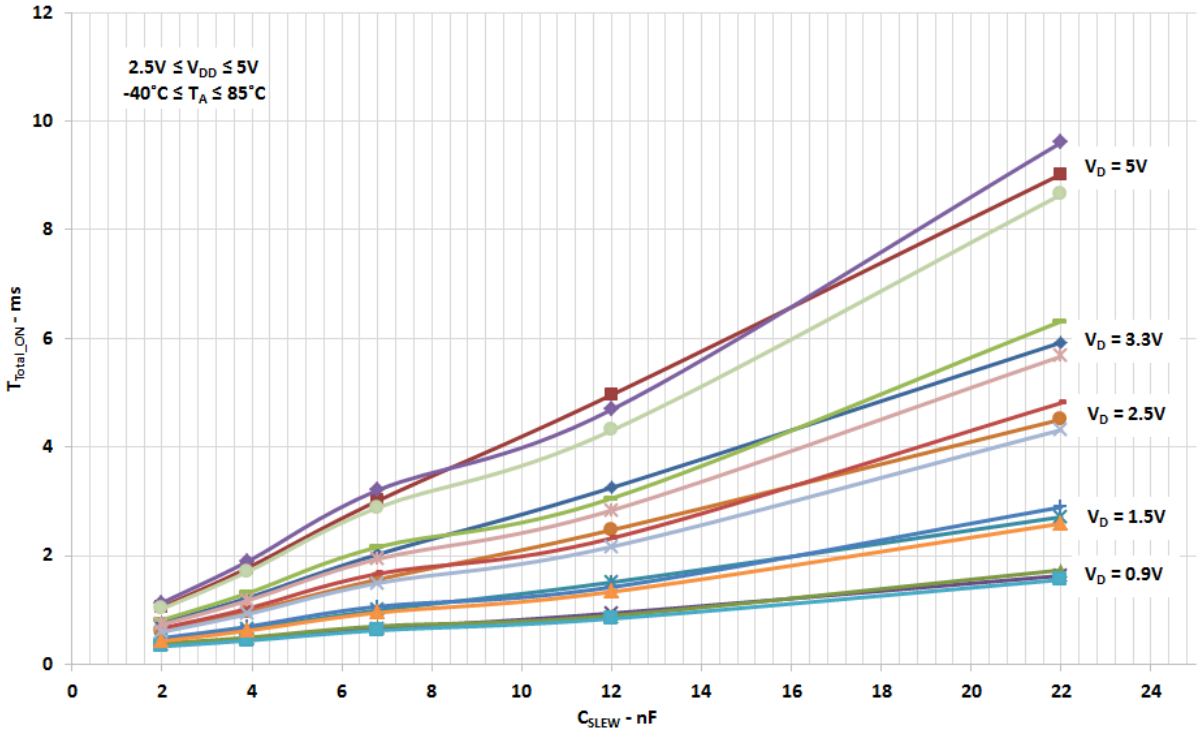
V_{OUT} Slew Rate vs. C_{SLEW}, V_{DD}, and Temperature



V_{OUT} Slew Rate vs. Temperature, V_{DD}, and C_{SLEW}



T_{Total_ON} vs. C_{SLEW}, V_D, and V_{DD}



Typical Turn-on Waveforms - V_{DD} = V_D = 5 V

ON

V_S

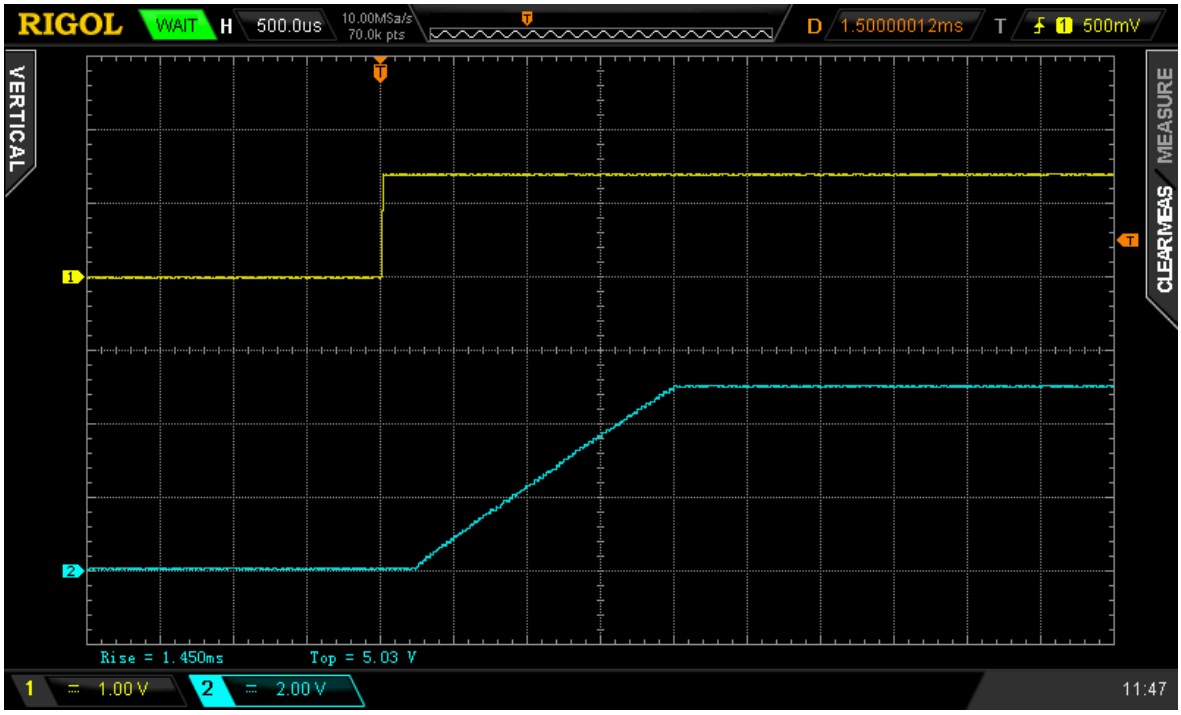


Figure 1. Typical Turn ON operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 4 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

ON

V_S

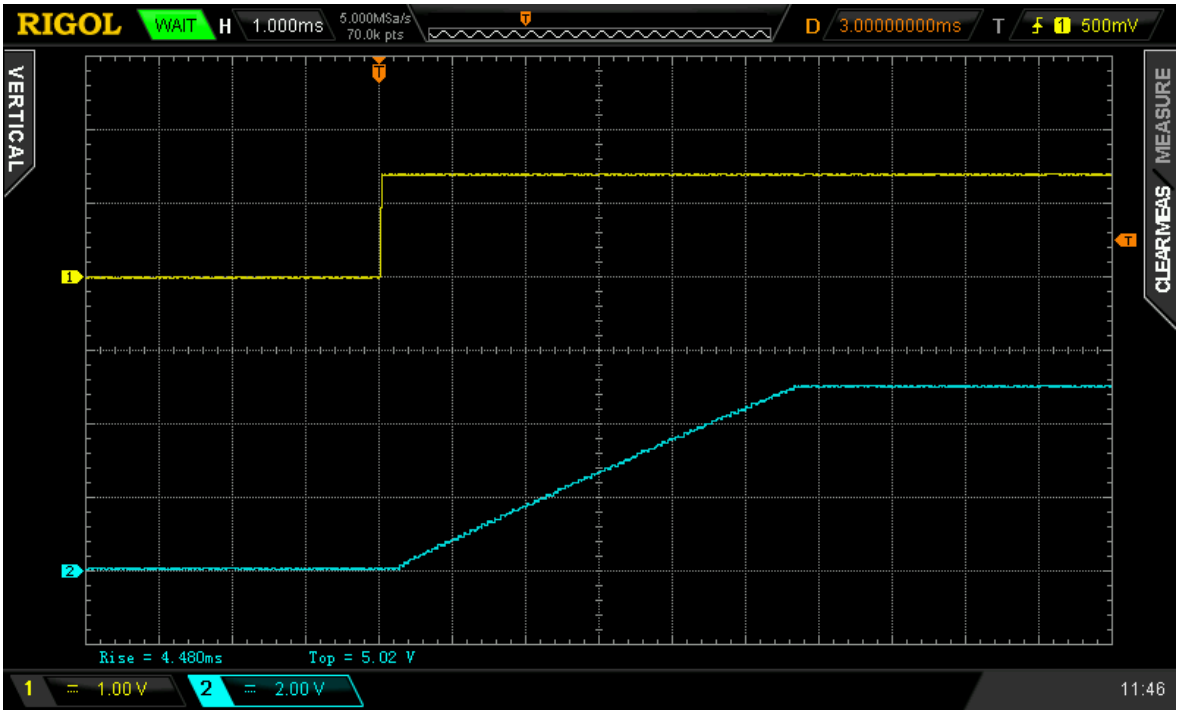


Figure 2. Typical Turn ON operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 12 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

Typical Turn-off Waveforms - V_{DD} = V_D = 5 V

ON

V_S

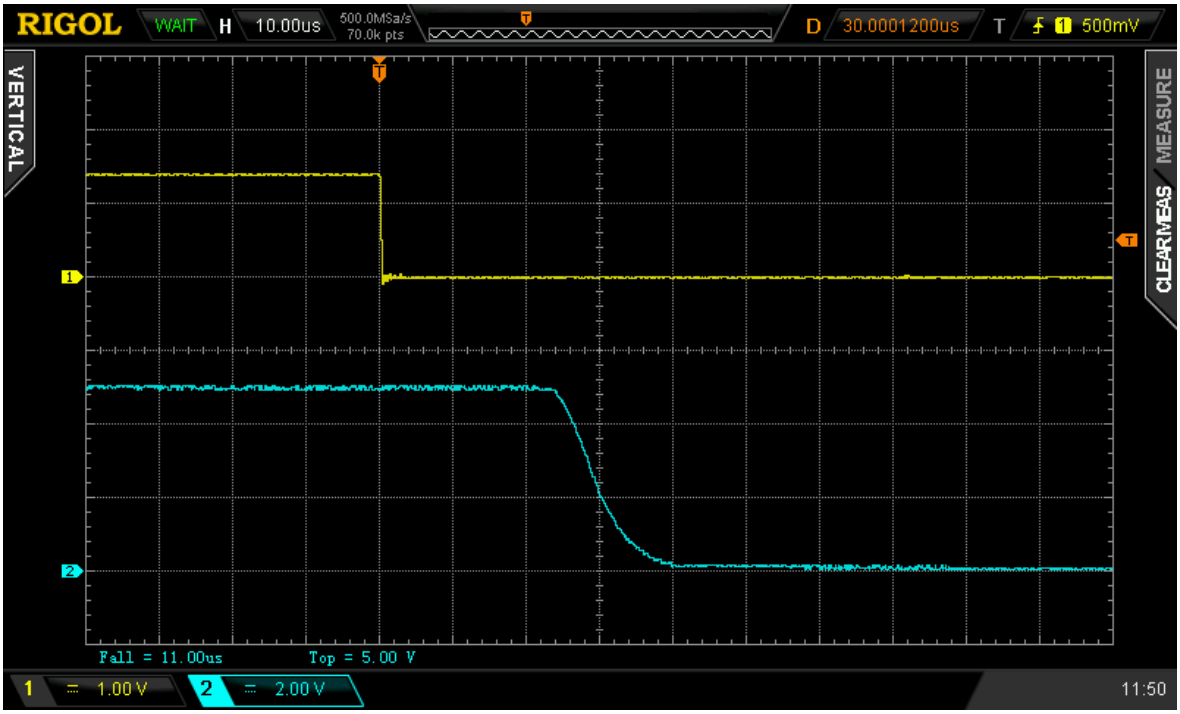


Figure 3. Typical Turn OFF operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 4 nF, no C_{LOAD}, R_{LOAD} = 20 Ω

ON

V_S

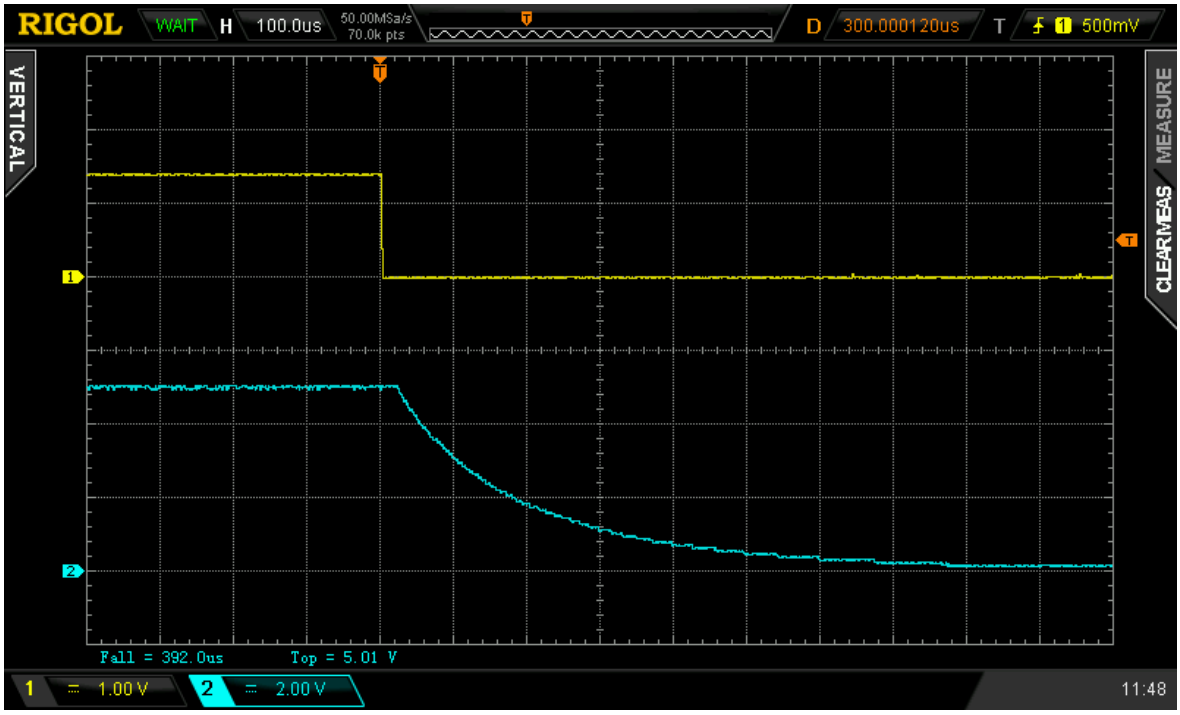


Figure 4. Typical Turn OFF operation waveform for V_{DD} = V_D = 5 V, C_{SLEW} = 4 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

SLG59M1735C Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1735C Voltage Limitation

V_D may not exceed V_{DD} for proper operation otherwise the Active Current Limit cannot function properly.

SLG59M1735C Current Limiting

The SLG59M1735C has two modes of current limiting, differentiated by the output (Source pin) voltage.

1. Standard Current Limiting Mode (with Thermal Protection)

When V_S > 250 mV, the output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceedng the Active Current Limit.

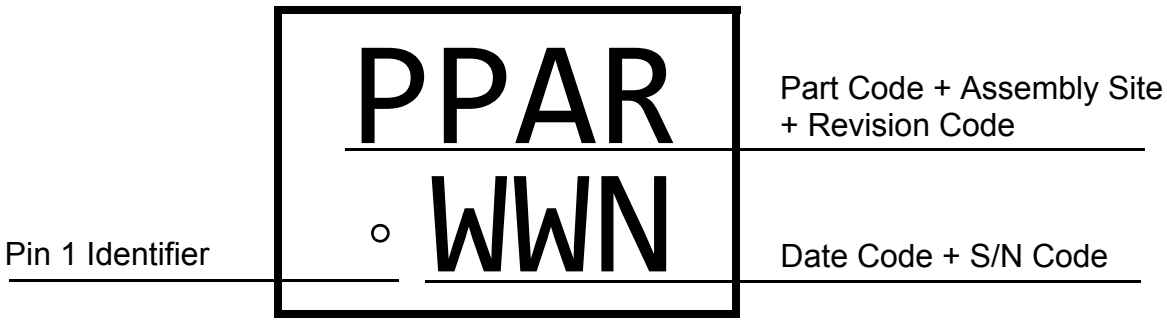
However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the $THERM_{ON}$ specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the $THERM_{OFF}$ temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

2. Short Circuit Current Limiting Mode (with Thermal Protection)

When V_S < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the current is limited to approximately 500 mA. Thermal Protection is also present, but since the Short Circuit Current Limit is much lower than Standard Current Limit, activation may only occur at higher ambient temperatures.

For more information on Silego GreenFET3 integrated power switch features, please visit our Application Notes page at our website and see App Note “AN-1068 GreenFET3 Integrated Power Switch Basics”.

Package Top Marking System Definition

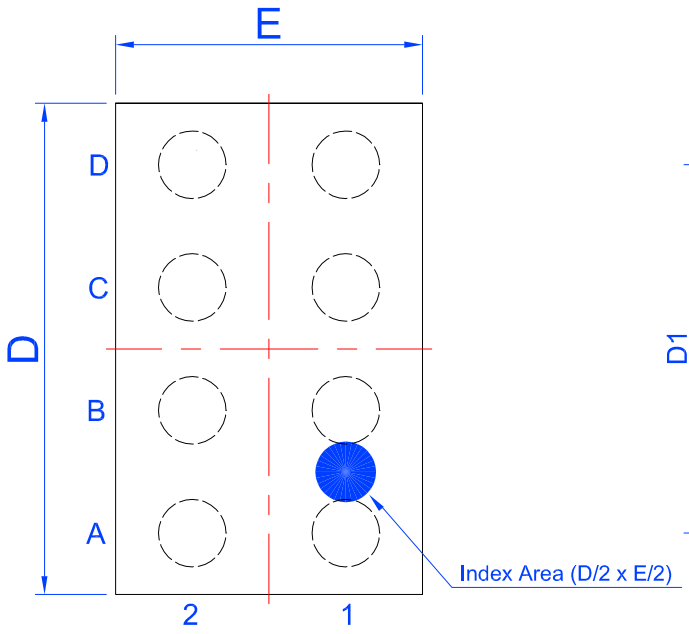


PP - Part Code Field
A - Assembly Site Code Field
R - Revision Code Field
WW - Lot Traceability Field
N - S/N Code Field

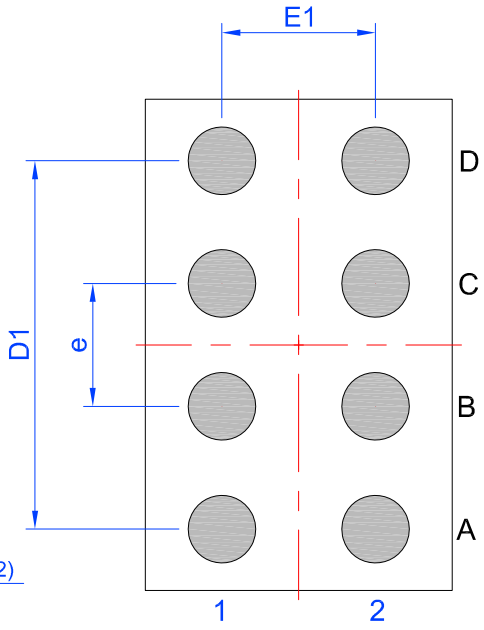
Package Drawing and Dimensions

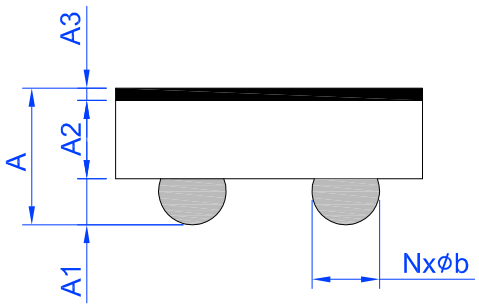
WLCSP 8L 0.96x1.56 mm 0.4P Green Package

Laser Marking View



Bump View





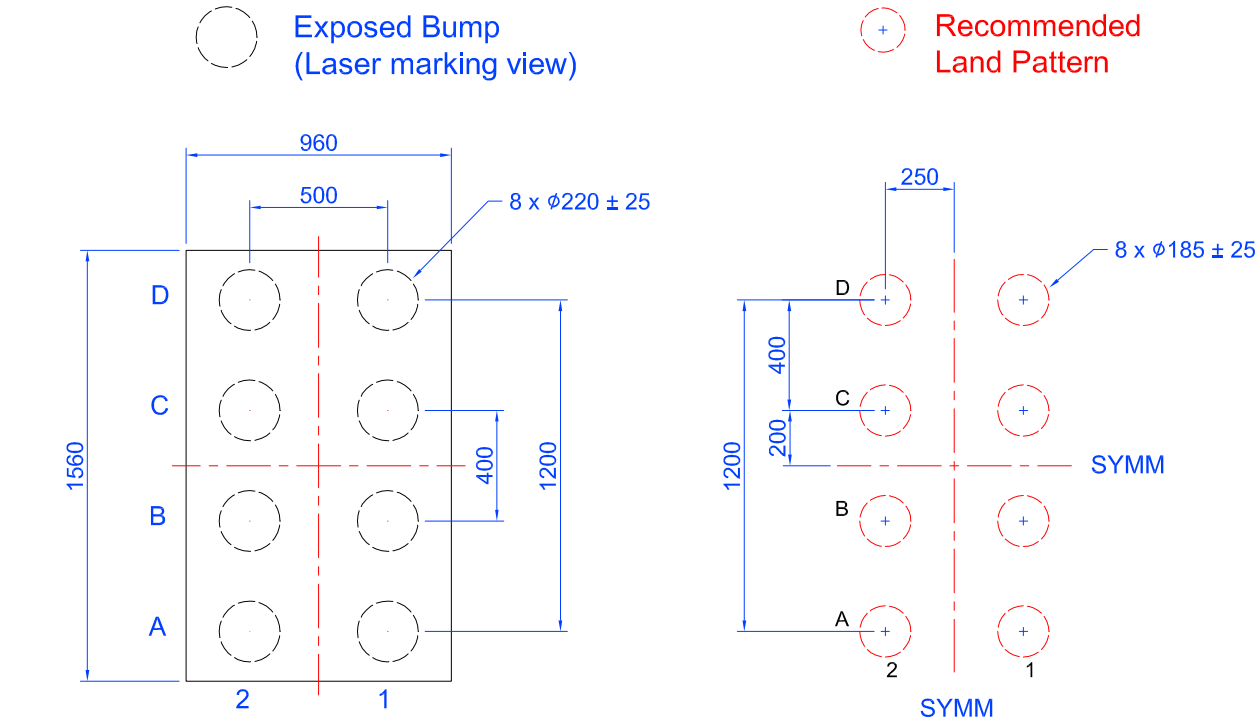
SIDE View

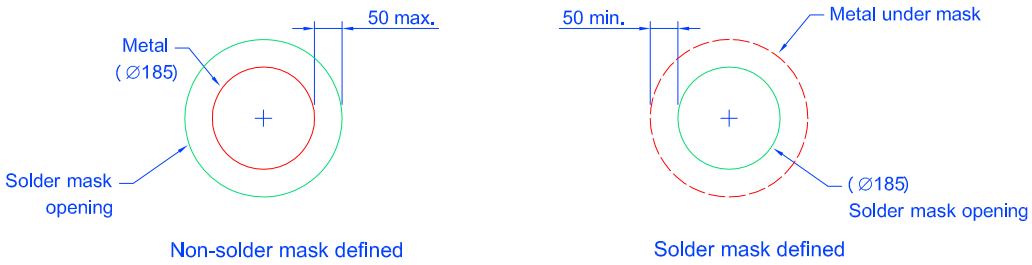
PIN No	PIN NAME
A1	VDD
A2	GND
B1	ON
B2	CAP
C1	MOS_D
C2	MOS_S
D1	MOS_D
D2	MOS_S

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.380	-	0.500	D	1.53	1.56	1.59
A1	0.125	0.150	0.175	E	0.93	0.96	0.99
A2	0.240	0.265	0.290	D1	1.20 BSC		
A3	0.015	0.025	0.035	E1	0.50 BSC		
b	0.195	0.220	0.245	e	0.40 BSC		
N	8 (Bump)						

SLG59M1735C 8-pin WLCSP PCB Landing Pattern



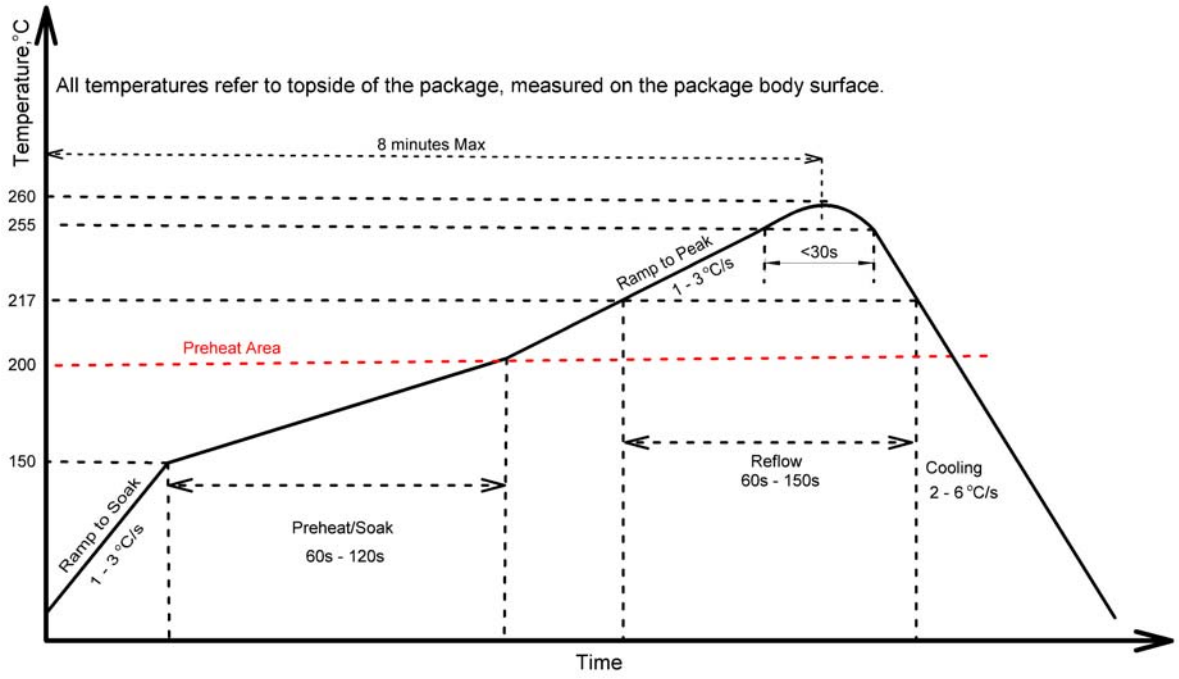


Solder mask detail (not to scale)

Unit: um

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1735C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

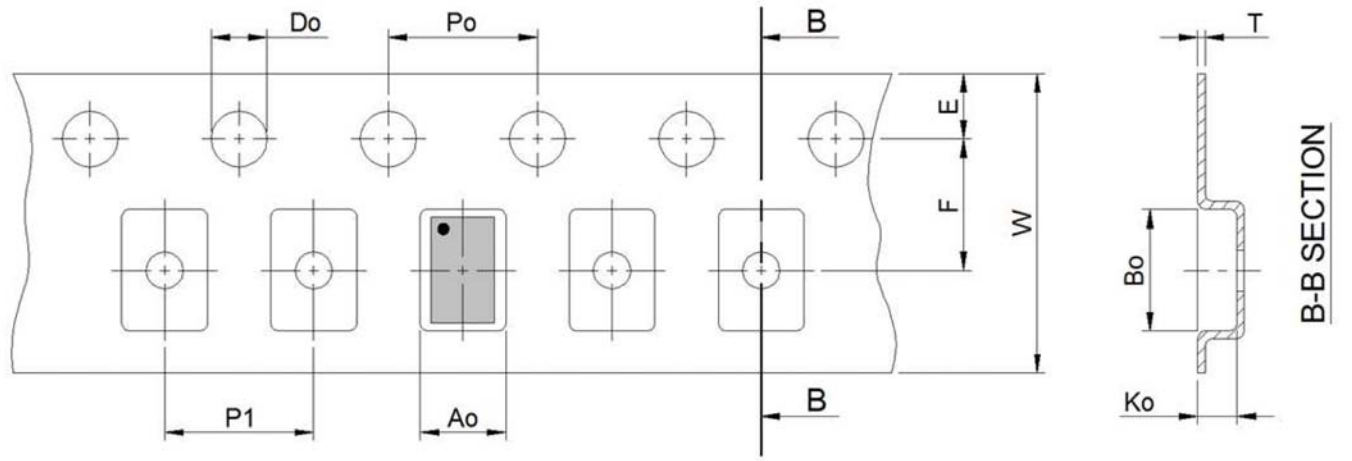
Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.352 mm^3 (nominal).Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm^3 (nominal).

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 8L 0.96x1.56 mm 0.4P Green	8	0.96 x 1.56 x 0.44	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 8L 0.96x1.56 mm 0.4P Green	1.11	1.7	0.56	4	4	1.5	1.75	3.5	8	0.25



Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Refer to EIA-481 specification

Revision History

Date	Version	Change
8/11/2017	1.02	Updated Tape and Reel Specs
3/28/2017	1.01	Updated PCB Landing Pattern
2/1/2017	1.00	Production Release